Schematic Design Review checklists

|  |  |
| --- | --- |
| Part / Assembly | P-1000072 |
| Revision |  |
| Review Date |  |
| Review Type |  |
| Reviewed By |  |

# Schematic Review

|  |  |  |  |
| --- | --- | --- | --- |
| # | Check | Completed | Comment |
|  | **Individual Components** |  |  |
|  | Component links match footprint and annotations |  |  |
|  | All nets are limited to below the max V, I etc of the component | Y |  |
|  | Adequate filtering is provided where needed. Consider ferrites, series resistors and TVS on signals going externally. Consider filtering on power lines, esp is low noise power is needed for analog signals | y |  |
|  | Race conditions checked | y |  |
|  | Starts up into known/controlled state | y |  |
|  | Layout notes are present where required | y |  |
|  | Differential pairs specified where necessary | y |  |
|  | Compare to ref. design if available | y |  |
|  | All pins connected to sensible things | y |  |
|  | Polarisation checked | y |  |
|  |  |  |  |
|  | **Power Lines** |  |  |
|  | Input power lines fused and protected | na |  |
|  | For automotive use, Two ceramic capacitors placed in series across input lines and at right angles to each other. | na |  |
|  | Power limiting behaviour verified | na |  |
|  | Power supplies are adequate | y |  |
|  |  |  |  |
|  | **IO** |  |  |
|  | Check pinouts for all external connectors match the connector they mate with | y |  |
|  | All outside lines filtered for RFI | y |  |
|  | All necessary lines protected against static discharge | y |  |
|  |  |  |  |
|  | **Other** |  |  |
|  | Overview sheet is present | na |  |
|  | Behaviour of entire schematic as expected | y |  |
|  | No 4 way joins, all other nets are joined where they should be | y |  |
|  | Test points where required | y |  |
|  | Signal LEDs where required | y |  |
|  | Debug headers for signals that may need external access | y |  |
|  | Confirm I2C has pull ups | na |  |
|  | Confirm Tx/Rx nets swapped as necessary (for UART, PCIe, etc etc) | y |  |
|  |  |  |  |
|  | **Component Selection** |  |  |
|  | Temp Grade |  |  |
|  | Ratings (eg automotive) |  |  |
|  | Suitable Functionality |  |  |
|  | Thermal Dissipation |  |  |
|  | Thermal Derating |  |  |
|  | Current Handling |  |  |
|  | Voltage |  |  |
|  | DC Bias (Cap and Inductor) |  |  |
|  | DNPs |  |  |
|  |  |  |  |

# Review Area

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| # | Sheet | Component/Net | Type | Comment | Recommended action | Designers response /action taken | Review Response | Designers response /action taken 2 |
|  |  | All |  | Sch isn’t readable in some areas. Sch should be super easy to ready, it’s purpose is to convey the function of the circuit as quickly, easily, and unambigiously to the ready as possible | No overlapping text, good spacing, minimise unlinked net label etc | Done | Looks ok, more spacing never really hurts. Also making sure labels are in consistent location and orientation makes things more readable. |  |
|  |  | R7/R10 |  | Do we need these? I think they will just mess up the signal path? |  |  | ok |  |
|  |  | L3/L4 |  | Should these be between caps and U2, or should the caps be between U2 and L3/4? |  | I have followed the reference design, which chee has used for review, but it was not using the same IC though | ok |  |
|  |  | U3 |  | Add decoupling caps next to U3 | I would add a couple of 1uF and 0.1uF caps next to ESP-07S VCC | Added | ok |  |
|  |  | U3 |  | U3 EN signal should have 0R resistor |  | Followed ESPWROOM-02U datasheet and added RC network, as it was recommended | ok |  |
|  |  | U3 |  | Add a series 22R or 100R resistor to the UART Tx and Rx lines. These can be used to improve signal quality and to protect the device in case of MCU failure or something |  | Done  Looks like it’s been taken care on MCU side | ok |  |
|  |  | VCC |  | Rename VCC net to 3V3 |  | Done | ok |  |
|  |  | 5v |  | Rename to 5V0 |  | Done | Missed one lower case ‘v’ 3v3 on U3 EN pin |  |
|  |  | U1 |  | Add output current rating next to output (800mA?) |  | Done | ok |  |
|  |  | J1 |  | Change name of 3v3 to indicate it is only for level shifting purposes |  | Done | ok |  |
|  |  | Electrical Char section |  | This is awesome, I would rename it power consumption, Add the 800mA output limit of the HX3406, (and possibly put it down near the PSU section?) |  | Done | ok |  |
|  |  | U2 |  | Was there an app not for this chip that you referenced? |  | I have followed the reference design, which chee has used for review, but it was not using the same IC though. <https://okrasolar.slack.com/archives/CERGXCN8K/p1629262801000400?thread_ts=1629091767.000800&cid=CERGXCN8K> | ok |  |
|  |  | D1 |  | Adding ESD diode is a very good call (the SE2604L states it is an ESD sensitive device). Should we add one to the RF input as well? (most assembly should be in ESD safe env, but given this is an oen source design it might be better same than sorry |  | Done | Ok. I’m not sure if we will want to load the 100pf caps on the rf lines.. Are they part of the App note? |  |
|  |  | U2/R11 |  | We should add a DNP 1k pull up resistor here as well in case we just want to have it enable all the time.  U2 also has a build in 10k pull down on the pin so we could possible get rid of R11 (or at least DNP) |  | Done | ok |  |
|  |  | TP30 |  | I would put the pair of bottom side (and one top side) GND test points in the power section as they are one of the “Power” nets |  | TP30 is not a ground | There are a bunch of GND test points on the GND pins from each IC, I would suggest putting the power test points in the power section for clarity? |  |
|  |  | U2 |  | Add a layout note saying that the RF path needs to be single ended 50R controlled impedance tracks, and that the tracs should be as should as possible and follow RF layout best practice. |  | Will do while working on layout | Can we add the note to the Sch? The idea is to have the layout note on the Sch so that if someone else needs to make layout changes later they have all the needed info. |  |
|  |  | Logos |  | Can we add an open hardware logo? |  | Not sure what I should do here! | Low priority, don’t worry about it |  |
|  |  | D1 |  | Value should be set to MPN |  | Done |  |  |
|  |  | J3 Host connector |  | Pin14 in NC on edamame. |  | Move mode select to pin 15 (nCS pin on edamame) |  |  |
|  |  | U1 Pin 5 |  | 4-way ‘+’ net connection off U1 pin 5 is not recommended as the circle can hide a missed connection. |  | Change it to two three way ‘T’ joins |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |